ABSTRACT OF THE DISCLOSURE

This invention has as its object to suppress an increase in circuit scale and to simplify a circuit structure by executing a filter process using a plurality of arithmetic units each of which makes multiplication and addition.

To achieve this object, image data Yn+2, Yn+3, and Yn+4 to be processed are read out (S2901), and three lattice point data d'n+1, S'n, and dn-1 are respectively read out from sequences H1, H2, and H3 corresponding to line buffers that store the lattice point data (S2903). $d'n+3 = Yn+3 + \alpha \cdot (Yn+2 + Yn+4)$ is computed (S2905), and d'n+3 is stored in the sequence H1 (S2907). $S'n+2 + \beta \cdot (d'n+1 + d'n+3)$ is computed (S2909), and S'n+2 is stored in the sequence H2 (S2911). $d'n+1 = d'n+1 + \gamma \cdot (S'n+2 + S'n)$ is computed (S2913), and dn+1 is stored in the sequence H3 (S2915). $Sn = S'n + \delta \cdot (dn-1 + dn+1)$ is computed (S2917), and Sn and dn+1 are output to the next processing stage (S2919).